CLAIMS

What is claimed is:

1. A transistor structure comprising:

a) a central channel region comprising a first semiconductor lightly doped with a first impurity element to increase first conductivity free carriers;

b) a source region and a drain region on opposing sides of the central channel region, both source region and the drain region being the first semiconductor heavily doped with the first impurity element;

c) a gate adjacent the channel region and forming a junction with the channel region, the gate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

2. The transistor structure of claim 1, further including a backgate adjacent the channel region, and on an opposing side of the channel region from the gate, and forming a junction with the channel region, the backgate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

3. The transistor structure of claim 2, wherein the fist semiconductor is silicon.

4. The transistor structure of claim 3, wherein the second semiconductor is carbon and the first and second semiconductor form a silicon carbide crystal structure.

5. The transistor structure of claim 4, wherein the first conductivity free carriers are electrons and the second conductivity free carriers are holes.

6. The transistor structure of claim 5, wherein the first impurity is arsenic.

7. The transistor structure of claim 6, wherein the second impurity is boron.

8. A silicon on insulator transistor structure comprising:

a) an insulating oxide layer separating a device layer of semiconductor material from a bulk semiconductor base region;

b) a generally rectangular central channel region within the device layer semiconductor material doped with a first impurity element to increase first conductivity free carriers;

c) a source region and a drain region on opposing sides of the generally rectangular central channel region, both the source region and the drain region comprising the device layer semiconductor material heavily doped with the first impurity element;

d) a gate adjacent the channel region and extending along a side of the central channel region adjacent the source region and forming a junction with the channel region, the gate comprising the device layer semiconductor and a second semiconductor with an energy gap greater than the device layer semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

9. The silicon on insulator transistor structure of claim 8, further including a backgate adjacent the channel region, and on an opposing side of the channel region from the gate, and forming a junction with the channel region, the backgate comprising the device layer semiconductor and a second semiconductor with an energy gap greater than the device layer semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

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10. The silicon on insulator transistor structure of claim 9, wherein the fist semiconductor is silicon.

11. The silicon on insulator transistor structure of claim 10, wherein the second semiconductor is carbon and the first and second semiconductor form a silicon carbide crystal structure.

12. The silicon on insulator transistor structure of claim 11, wherein the first conductivity free carriers are electrons and the second conductivity free carriers are holes.

13. The silicon on insulator transistor structure of claim 12, wherein the first impurity is arsenic.

14. The silicon on insulator transistor structure of claim 13, wherein the second impurity is boron.

15. A method of controlling the flow of electricity between a source semiconductor region and a drain semiconductor region, both heavily dopes with a first impurity element, the method comprising:

a) positioning a generally rectangular central channel region between the source region and the drain region, the channel region lightly doped with the first impurity element to increase free carriers of a first type;

b) positioning a gate adjacent the channel region and extending along a side of the central channel region adjacent the source region and forming a junction with the channel region, the gate comprising the semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase free carriers opposite of the first type; and

c) varying the potential of the gate region relative to the source region to control depletion within the channel region.

16. The method of controlling the flow of electricity of claim 15, further including:

d) positioning a backgate adjacent the channel region, and on an opposing side of the channel region from the gate, and forming a junction with the channel region, the backgate comprising the semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase free carriers opposite of the first type; and

e) varying the potential of the backgate relative to the source region to control depletion within the channel region.

17. The method of controlling the flow of electricity of claim 16, wherein the fist semiconductor is silicon.

18. The method of controlling the flow of electricity of claim 17, wherein the second semiconductor is carbon and the first and second semiconductor form a silicon carbide crystal structure.

19. The method of controlling the flow of electricity of claim 18, wherein the first conductivity free carriers are electrons and the second conductivity free carriers are holes.

20. The method of controlling the flow of electricity of claim 19, wherein the first impurity is arsenic.

21. The method of controlling the flow of electricity of claim 20, wherein the second impurity is boron.

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